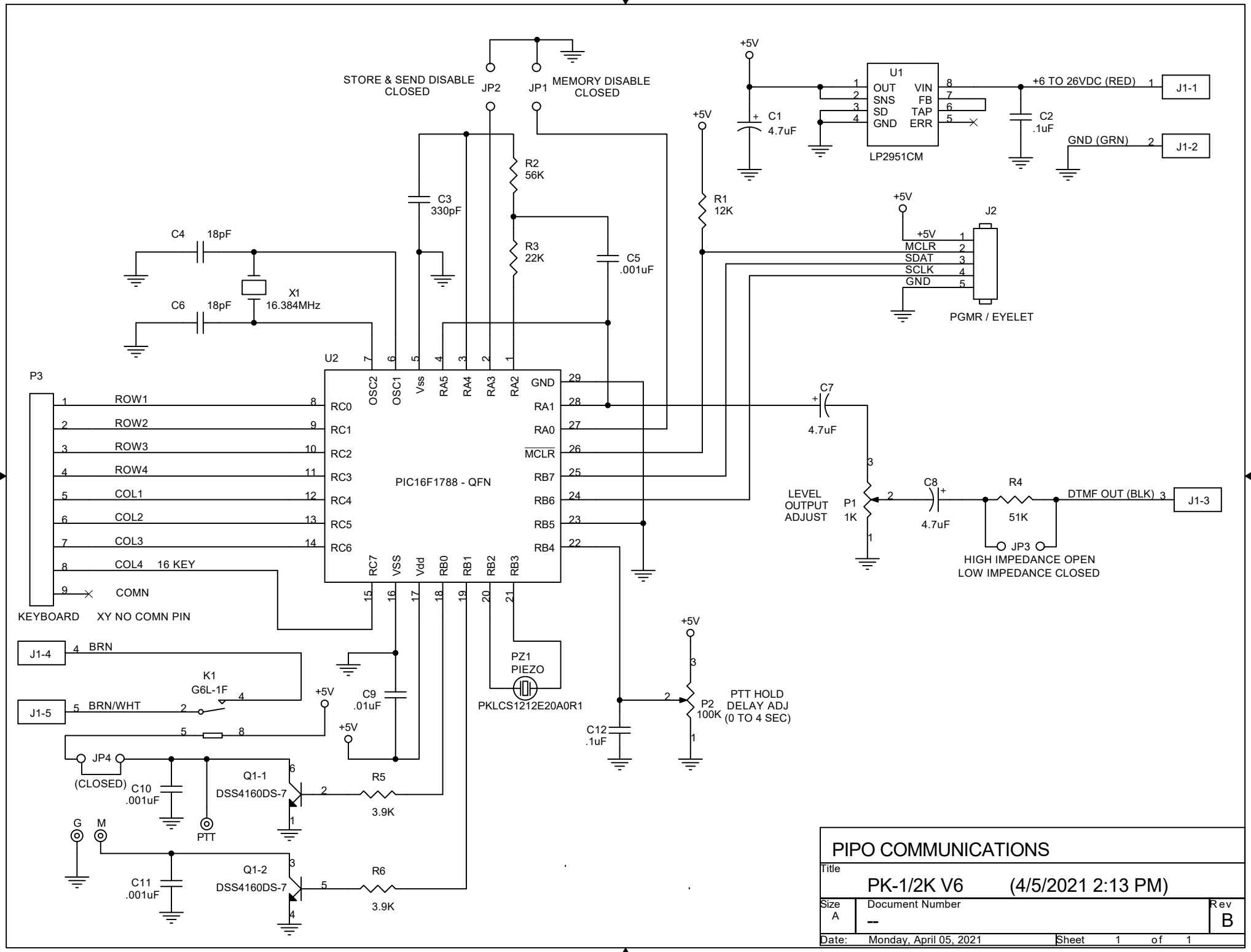
STORE & SEND DISABLE CLOSED
JP2
JP1
MEMORY DISABLE CLOSED
+5V
U1
OUT
SNS
SD
GND
VIN
FB
TAP
ERR
LP2951CM
C1
4.7uF
C2
.1uF
+6 TO 26VDC (RED)
J1-1
GND (GRN)
J1-2
R2
56K
R3
22K
C3
330pF
C5
.001uF
R1
12K
C4 18pF
C6 18pF
X1
16.384MHz
J2
MCLR
SDAT
SCLK
GND
PGMR / EYELET
U2
PIC16F1788 - QFN
OSC2
OSC1
Vss
RA5
RA4
RA3
RA2
RC0
RC1
RC2
RC3
RC4
RC5
RC6
RA1
RA0
MCLR
RB7
RB6
RB5
RB4
RC7
VSS
Vdd
RB0
RB1
RB2
RB3
P3
ROW1
ROW2
ROW3
ROW4
COL1
COL2
COL3
COL4
16 KEY
COMN
KEYBOARD
XY NO COMN PIN
C7
4.7uF
LEVEL OUTPUT ADJUST
P1
1K
C8
4.7uF
R4
51K
DTMF OUT (BLK)
J1-3
JP3
HIGH IMPEDANCE OPEN
LOW IMPEDANCE CLOSED
J1-4
BRN
J1-5
BRN/WHT
K1
G6L-1F
C9
.01uF
PZ1
PIEZO
PKLCS1212E20A0R1
C12
.1uF
P2
100K
PTT HOLD DELAY ADJ (0 TO 4 SEC)
JP4
(CLOSED)
C10
.001uF
Q1-1
DSS4160DS-7
R5
3.9K
PTT
G
M
C11
.001uF
Q1-2
DSS4160DS-7
R6
3.9K
PIPO COMMUNICATIONS
Title
PK-1/2K V6 (4/5/2021 2:13 PM)
Size
A
Document Number
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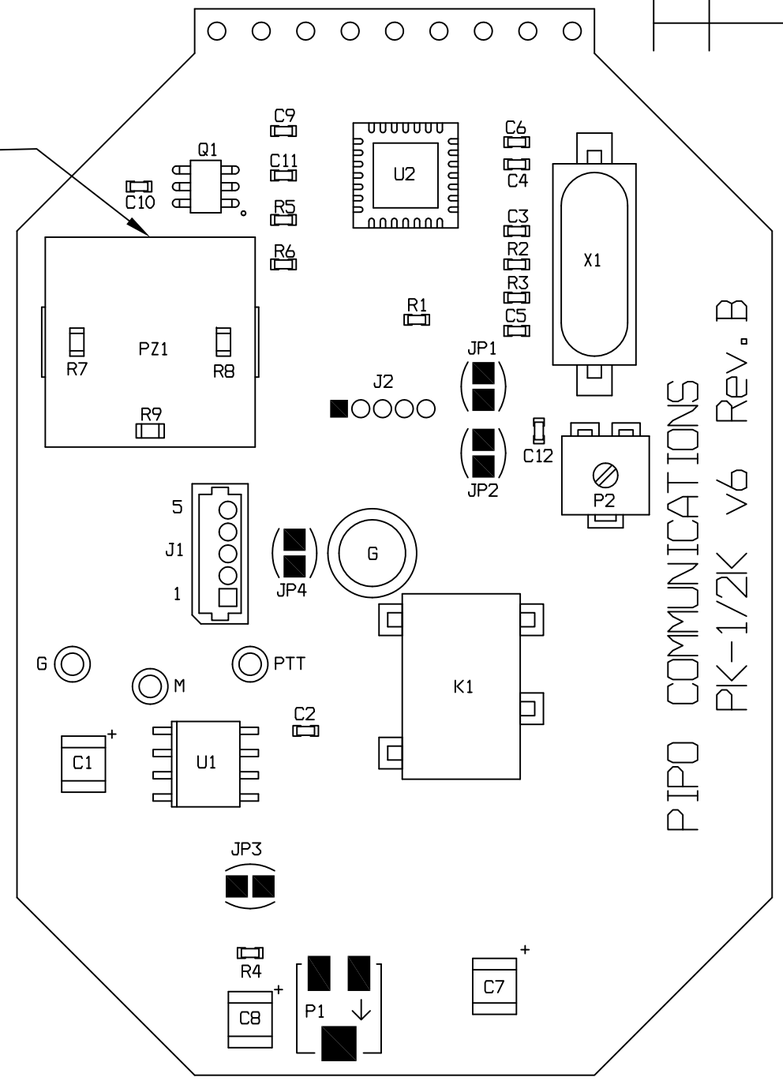
Rev
B
Date: Monday, April 05, 2021
Sheet 1 of 1

REVISIONS		
DESCRIPTION	DATE	APPROVED

PZ1, SOUND EMITTING HOLE, BOTTOMSIDE



5. J2, 9 HOLES AT TOP OF BOARD, "M", "G", AND "PTT" ARE HOLES ARE TO BE VOID OF SOLDER.
4. R7, R8 AND R9 ARE USED AS SPACERS TO INSTALL PZ1. PZ1 IS INSTALLED BY HAND. IT IS NOT SEALED.
3. DO NOT INSTALL THE FOLLOWING COMPONENTS: J2, JP1–JP4,
2. INSTALL COMPONENTS, MAKE ALL INTERFACIAL CONNECTIONS, ASSEMBLE AND SOLDER IAW J–STD–001, CLASS 2.
1. SEE SEPARATE PARTS LIST FOR COMPONENT VALUE AND/OR USAGE.

NOTES: UNLESS OTHERWISE SPECIFIED.

UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES TOLERANCES ARE:

DECIMALS	ANGLES
.X = ± .1	
.XX = ± .03	± 0°30′
.XXX = ± .005	

DO NOT SCALE DRAWING

TREATMENT

FINISH

CONTRACT NO.

APPROVALS	DATE
DWN. R. GONZALES	9/26/2018
CHK.	
ENG.	
APP.	

THIS DRAWING PRODUCED BY: P.C.D.C.
FILE: PK–1–2K v6_B ASSY

PIPO COMMUNICATIONS
HOLLYWOOD, CALIFORNIA

TITLE
PCB ASSEMBLY:
PK–1/2K v6

SIZE	CAGE CODE	DWG NO.	REV
B			B

SCALE 3 : 1 | 9/26/2018 9:18 PM | SHEET 1 OF 1